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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 08/917,003
Priority Filing Date ....August 20, 1997
Inventor .... Kie Y. Ahn
Assignee... Micron Technology, Inc.
Priority Group Art Unit 2823
Priority Examiner .... K. Eaton
Attorney's Docket No. MI22-1738
Title: Conductive Lines, Coaxial Lines, Integrated Circuitry, and Methods of Forming Conductive Lines, Coaxial Lines, and Integrated Circuitry

PRELIMINARY AMENDMENT

To: Assistant Commissioner for Patents
Washington, D.C. 20231

From: Frederick M. Fliegel, Ph.D.
(Tel. 509-624-4276; Fax 509-838-3424)
Wells, St. John, Roberts, Gregory & Matkin P.S.
601 W. First Avenue, Suite 1300
Spokane, WA 99201-3817

Sir:

This is a preliminary amendment accompanying a Request for Divisional Application for the above-entitled patent application. Prior to examining the application, please enter the following amendments.

AMENDMENTS

In the Specification

At page 1, after the title, insert:

CROSS REFERENCE TO RELATED APPLICATION

This patent application is a Continuation Application of U.S. Patent Application Serial No. 08/917,003, filed August 20, 1997, entitled "Conductive Lines, Coaxial Lines, Integrated Circuitry, and Methods of Forming Conductive Lines, Coaxial Lines, and Integrated Circuitry", naming Kie Y. Ahn as inventor.

Replace the paragraph beginning on page 1, line 20, and extending through p. 2, line 8, with:

Conductive lines, such as co-axial lines, integrated circuitry incorporating such conductive lines, and methods of forming the same are described. In one aspect, a substrate having an outer surface is provided. A masking material is formed over the outer surface and subsequently patterned to form a conductive line pattern. An inner conductive layer is formed within the conductive line pattern, followed by formation of a dielectric layer thereover and an outer conductive layer over the dielectric layer. Preferred implementations include forming the inner conductive layer through electroplating, or alternatively, electroless plating techniques. Other preferred implementations include forming the dielectric layer from suitable polymer materials having desired dielectric properties. A vapor-deposited dielectric layer of parylene is one such preferred dielectric material.

Replace the paragraph beginning at p. 4, line 8 and extending through p. 4, line 17, with the paragraph shown below.

Referring to Fig. 2, conductive terminal members 20, 22, and 24 are formed over outer surface 18. Such constitute exemplary respective node locations with which electrical connection or communication is desired. In accordance with one aspect of the invention, other conductive terminal members are formed over the substrate and extend into and out of the plane of the page upon which Fig. 2 appears. Such other conductive terminal members can form, together with the illustrated terminal members, respective pairs of upstanding, spaced-apart terminal members. One such exemplary pair is shown in Fig. 12 at 20, 21 and discussed in more detail below.

Replace the paragraph beginning at p. 5, line 1 and extending through p. 5, line 20, with the paragraph shown below.

Referring to Fig. 4, first layer 26 is patterned over outer surface 18 to form at least one, and preferably a plurality, of conductive line patterns 28, 30, and 32. In one aspect, conductive line patterns 28, 30, and 32 expose at least portions of respective conductive terminal members 20, 22, and 24 and their respective mated terminal members which define the respective pairs of upstanding terminal members mentioned above. Ideally, and with reference to Fig. 5, this forms a trough 23 through first layer 26 which extends between and joins respective terminal member pairs such as exemplary pairs 20, 21. Yet, trough 23 does not extend to surface 18. Such can be accomplished by limiting the time of light exposure of the preferred photoresist of layer 26 such

that only an outermost portion is light transformed for subsequent stripping. Alternately, where layer 26 constitutes another material such as SiO_2, the formation of a trough between the silicon pairs in a manner which avoids surface 18 exposure could be achieved with a masked timed etch. An etch stop layer might also be used. Regardless, the trough formation enables the spaced-apart conductive terminal members, such as terminal members 20, 21, to be electrically connected through the respective conductive line patterns, as will become apparent below.

Replace the paragraph beginning at p. 8, line 1 and extending through p. 8, line 21, with the paragraph shown below.

Referring to Fig. 10, a dielectric layer 44 is formed over substrate 16 and at least some of the inner conductive layers comprising respective conductive lines 38, 40, and 42. Preferably, layer 44 comprises a dielectric polymer layer which is formed over and surrounds at least the respective portions of conductive lines 38, 40, and 42 which are spaced from outer surface 18 and extend between the terminal members. An example material is parylene. Parylene desirably has a lower dielectric constant, e.g. 2.6, as compared with dielectric constants of other materials such as SiO_2 which can have dielectric constants from between 3.9 to 4.2. Such accommodates operating parameters of high speed integrated circuitry by increasing signal propagation (decreasing propagation times) and reducing interline coupling or crosstalk. The preferred parylene material is preferably vapor phase deposited over the substrate and the respective conductive lines. Parylene

and processing techniques which utilize parylene are described in more detail in an article entitled "Low and High Dielectric Constant Thin Films for Integrated Circuit Applications", authored by Guttman et al., and presented to the Advanced Metallization and Interconnect Systems for VLSI Applications in 1996, held in Boston, Massachusetts, October 3-5, 1996, and published in May/June 1997 by Material Research Society of Pittsburgh, Pa.

In the Claims

Please cancel claims 1-34 without prejudice, amend claims 35-37 and add new claims 38-62 as shown below.

35. (Amended) Integrated circuitry comprising:

a semiconductive substrate having an outer surface;

an inner conductive core spaced from and suspended over the outer surface;

a polymer dielectric layer surrounding a substantial portion of the inner conductive core; and

an outer conductive sheath surrounding a substantial portion of the polymer dielectric layer.

36. (Amended) Integrated circuitry comprising:

a semiconductive substrate having an outer surface;

a pair of spaced-apart terminal members disposed over the outer surface and extending elevationally away therefrom;

an inner conductive core operably connected with and suspended between the spaced-apart terminal members above the outer surface;

a polymer dielectric layer over a substantial portion of the inner conductive core; and

an outer conductive sheath surrounding a substantial portion of the polymer dielectric layer.

37. (Amended) Integrated circuitry comprising:

a substrate having an outer surface;

a pair of upstanding, spaced-apart conductive terminal members disposed over the substrate outer surface;

a copper-comprising layer of material operably connected with and suspended above the outer surface between the terminal members, the copper-comprising layer having a thickness of between about 100 to 200 nanometers;

a conductive layer of material disposed over and operably connected with the copper-comprising layer of material, the conductive layer comprising conductive material selected from the group consisting of copper, gold, nickel, cobalt, and iron;

a dielectric layer comprising parylene disposed over the conductive layer of material, the dielectric layer surrounding conductive layer portions which extend between the terminal members; and

an outer conductive sheath of material disposed over the dielectric layer and surrounding dielectric layer portions which extend between the terminal members.

<u>**New Claims**</u>

38. The integrated circuitry of claim 35, wherein the outer conductive sheath leaves some void space between the outer conductive sheath and the outer surface.

39. The integrated circuitry of claim 35, wherein the outer conductive sheath is not formed on the outer surface.

40. The integrated circuitry of claim 35, wherein the polymer dielectric layer comprises parylene.

41. The integrated circuitry of claim 35, wherein the polymer dielectric layer has a relative dielectric constant of about 2.6.

42. The integrated circuitry of claim 35, wherein the outer conductive sheath comprises aluminum.

43. The integrated circuitry of claim 35, wherein the inner conductive core comprises copper.

44. The integrated circuitry of claim 35, wherein the inner conductive core comprises a material chosen from a group consisting of nickel, cobalt and iron.

45. The integrated circuitry of claim 36, wherein the polymer dielectric layer comprises parylene.

46. The integrated circuitry of claim 36, wherein the polymer dielectric layer has a relative dielectric constant of about 2.6.

47. The integrated circuitry of claim 36, wherein the outer conductive sheath comprises aluminum.

48. The integrated circuitry of claim 36, wherein the inner conductive core comprises copper.

49. The integrated circuitry of claim 36, wherein the inner conductive core comprises a material chosen from a group consisting of nickel, cobalt and iron.

50. Integrated circuitry comprising:

a semiconductive substrate having an outer surface;

an inner conductive core spaced from and over the outer surface;

a polymer dielectric layer surrounding a substantial portion of the suspended inner conductive core; and

an outer conductive sheath surrounding a substantial portion of the polymer dielectric layer, the outer conductive sheath leaving some void space between the outer conductive sheath and the outer surface, wherein the outer conductive sheath is not formed on the outer surface.

51. The integrated circuitry of claim 50, wherein the polymer dielectric layer comprises parylene.

52. The integrated circuitry of claim 50, wherein the polymer dielectric layer has a relative dielectric constant of about 2.6.

53. The integrated circuitry of claim 50, wherein the outer conductive sheath comprises aluminum.

54. The integrated circuitry of claim 50, wherein the inner conductive core comprises copper.

55. The integrated circuitry of claim 50, wherein the inner conductive core comprises a material chosen from a group consisting of nickel, cobalt and iron.

56. Integrated circuitry comprising:

a semiconductive substrate having an outer surface;

a pair of spaced-apart terminal members disposed over the outer surface and extending elevationally away therefrom;

an inner conductive core operably connected with and suspended between the spaced-apart terminal members above the outer surface;

a polymer dielectric layer surrounding the suspended inner conductive core; and

an outer conductive sheath surrounding a substantial portion of the polymer dielectric layer while some void space is present between the dielectric layer over the suspended inner conductive core and the outer

surface, the outer conductive sheath leaving some void space between the outer conductive sheath and the outer surface, wherein the outer conductive sheath is not formed over the substrate outer surface.

57. The integrated circuitry of claim 56, wherein the polymer dielectric layer comprises parylene.

58. The integrated circuitry of claim 56, wherein the polymer dielectric layer has a relative dielectric constant of about 2.6.

59. The integrated circuitry of claim 56, wherein the outer conductive sheath comprises aluminum.

60. The integrated circuitry of claim 56, wherein the inner conductive core comprises copper.

61. The integrated circuitry of claim 56, wherein the inner conductive core comprises a material chosen from a group consisting of nickel, cobalt and iron.

62. Integrated circuitry comprising:

a substrate having an outer surface;

a pair of upstanding, spaced-apart conductive terminal members disposed over the substrate outer surface;

a copper-comprising layer of material operably connected with and suspended above the outer surface between the terminal members, the copper-comprising layer having a thickness of between about 100 to 200 nanometers;

a conductive layer of material operably connected with the copper-comprising layer of material and suspended above the outer surface between the terminal members, the conductive layer comprising conductive material selected from the group consisting of copper, gold, nickel, cobalt, and iron;

a dielectric layer comprising parylene disposed over the conductive layer of material, the dielectric layer surrounding the suspended conductive layer portions ; and

an outer conductive sheath of material disposed over the dielectric layer and surrounding dielectric layer portions which extend between the terminal members, the outer conductive sheath leaving some void space between the outer conductive sheath and the outer surface, wherein the outer conductive sheath is not formed over the substrate outer surface.

REMARKS

This application is a divisional application of U.S. Patent Application Serial No. 08/917,003 and is being filed responsive to a restriction requirement therein. Accordingly, claims 1-34 have been canceled without prejudice, claims 35-37 have been amended and new claims 38-62 have been added. Claims 35-62 remain in the application for consideration.

New claims 38-62 and the amendments to the specification and claims are supported at least by text appearing at p. 3, line 21 through p. 9, line 14 of the application as originally filed. No new matter is added by new claims 38-62 or by the amendments to the specification and claims.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page(s) are captioned "**Version with markings to show changes made**."

This application is believed to be in condition for allowance and action to that end is requested. The Examiner is requested to telephone the undersigned in the event that the next office action is one other than a Notice of Allowance. The undersigned is available during normal business hours (Pacific Time Zone).

Respectfully submitted,

Dated: June 21, 2001

By: ______________________
Frederick M. Fliegel, Ph.D.
Reg. No. 36,138

Version with markings to show changes made.

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37 CFR §1.121(b)(1)(iii) AND 37 CFR §1.121(c)(1)(ii) FILING REQUIREMENTS TO ACCOMPANY PRELIMINARY AMENDMENT

Deletions are bracketed, additions are underlined.

In the Specification

At page 1, after the title insert:

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The paragraph beginning at p. 4, line 8 and extending through p. 4, line 17 has been amended as shown below.

Referring to Fig. 2, conductive terminal members 20, 22, and 24 are formed over outer surface 18. Such constitute exemplary respective node locations with which electrical connection or communication is desired. In accordance with one aspect of the invention, other conductive terminal members are formed over the substrate and extend into and out of the plane of the page upon which Fig. 2 appears. Such other conductive terminal

members can form, together with the illustrated terminal members, respective pairs of upstanding, spaced-apart terminal members. One such exemplary pair is shown in Fig. [11] 12 at 20, 21 and discussed in more detail below.

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The paragraph beginning at p. 8, line 1 and extending through p. 8, line 21 has been amended as shown below:

Referring to Fig. 10, a dielectric layer 44 is formed over substrate 16 and at least some of the inner conductive layers comprising respective conductive lines 38, 40, and 42. Preferably, layer 44 comprises a dielectric polymer layer which is formed over and surrounds at least the respective portions of conductive lines 38, 40, and 42 which are spaced from outer surface 18 and extend between the terminal members. An example material is [Parylene] parylene. Parylene desirably has a lower dielectric constant, e.g. 2.6, as compared with dielectric constants of other materials such as SiO_2 which can have dielectric constants from between 3.9 to 4.2. Such accommodates operating parameters of high speed integrated circuitry by increasing signal propagation (decreasing propagation times) and reducing interline coupling or crosstalk. The preferred [Parylene] parylene material is preferably vapor phase deposited over the substrate and the respective conductive lines. Parylene and processing techniques which utilize parylene are described in more detail in an article entitled "Low and High Dielectric Constant Thin Films for Integrated Circuit Applications", authored by Guttman et al., and presented to the Advanced Metallization and Interconnect Systems for VLSI Applications in 1996, held in Boston, Massachusetts, October 3-5, 1996, and published in May/June 1997 by Material Research Society of Pittsburgh, Pa.

<u>In the Claims</u>

Claims 1-34 have been canceled and claims 38-62 have been added. Claims 35-37 have been amended as shown below.

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a semiconductive substrate having an outer surface;

an inner conductive core spaced from and <u>suspended</u> over the outer surface;

a polymer dielectric layer surrounding a substantial portion of the inner conductive core; and

an outer conductive sheath surrounding a substantial portion of the polymer dielectric layer.

36. (Amended) Integrated circuitry comprising:

a semiconductive substrate having an outer surface;

a pair of spaced-apart terminal members disposed over the outer surface and extending elevationally away therefrom;

an inner conductive core operably connected with and [extending] <u>suspended</u> between the spaced-apart terminal members <u>above the outer surface</u>;

a polymer dielectric layer over a substantial portion of the inner conductive core; and

an outer conductive sheath surrounding a substantial portion of the polymer dielectric layer.

37. (Amended) Integrated circuitry comprising:

a substrate having an outer surface;

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a copper-comprising layer of material operably connected with and [extending] suspended above the outer surface between the terminal members, the copper-comprising layer having a thickness of between about 100 to 200 nanometers;

a conductive layer of material disposed over and operably connected with the copper-comprising layer of material, the conductive layer comprising conductive material selected from the group consisting of copper, gold, nickel, cobalt and iron;

a dielectric layer comprising [Parylene] parylene disposed over the conductive layer of material, the dielectric layer surrounding conductive layer portions which extend between the terminal members; and

an outer conductive sheath of material disposed over the dielectric layer and surrounding dielectric layer portions which extend between the terminal members.

END OF DOCUMENT